Arizona

Semi-annual Progress Report for Period 4/1/65 to 10/1/65

NASA Grant NsG-646 (Analog/hybrid Computer Study)

September 22, 1965

1. ASTRAC II System

Reference is again made to the description of the ASTRAC II computer in our status report of November 20, 1964 (ACL Memo No. 96). The partially completed ASTRAC II was demonstrated to a joint meeting of the Western and Rocky Mountain Simulation Councils in April; the audience include both NASA and USAF computer specialists as well as industry and university experts. The demonstration included digitally timed analog computation at 1 kc iteration rate, automatic time-scale switching, and computation of the impulse response of a 3 kc filter excited with pseudo-random noise through input-output crosscorrelation. ASTRAC II techniques also were the subject of an invited symposium paper at the May, 1965 IFIP Congress in New York.

The remainder of the report period (i.e., the Summer semester 1965) was spent on the construction of the remaining computer components (Maybach, Whigham). The machine now comprises

40 operational amplifiers (16 are integrator/track-hold units)
7 electronic multipliers
4 D/A converter multipliers
6 plug-in diode function generators
4 sine/cosine generators
6 fast comparators
40 coefficient potentiometers
1 Digital timer/control unit

N66-80135 (ACCESSION NUMBER) 4 (PAGES) CR-68043 (NASA CR OR TMX OR AD NUMBER) (THRU) None (CODE) (CATEGORY) FACILITY FORM 602

1 Free-digital-logic panel

1 Statistics computer

1 Optimizer panel

1 Pseudo-random-noise generator (28 shift-register stages)

1 Digital voltmeter

1 Binary A/D converter (to connect to a digital computer)

The machine is now computing and may be considered as completed as soon as its five analog patchboards are silk-screened on October 6. Components still to be added are

12 D/A switches

4 limiter modules (diode bridges and free diodes)

Checkout and accuracy tests are proceeding. The only real technical difficulty encountered was digital noise from the high-level logic (0 to -6V) cards used; future fast hybrid computers should surely employ integrated-circuit logic with low logic levels (0.6 to 1.6V). We were able to reduce analog-computer peak noise due to the digital modules from over 300 mV to 20 mV; rms noise is much smaller. The noise-reduction program is continuing,[2] with peak noise below 15 mV believed possible with the high-level logic.

ASTRAC II operating and maintenance manuals were started in draft form. Analog and digital patchbay designs were frozen after the first experiments with actual computations. All artwork is complete, and silk screening is scheduled for the first week of October.

2. ASTRAC II Component Development

R. Whigham improved the comparator and sine/cosine generator circuits developed in 1964, supervised the design of new D/A switches (also used in the new D/A converters), and increased the 0.5 per cent error frequency of our track-hold circuit from 10 kc to 20 kc. R. Maybach completely redesigned the ASTRAC II pseudo-random-noise generator for higher output and greatly improved setup convenience. E. O'Grady joined the optimizer unit (previously tried with ASTRAC I) to ASTRAC II; checkout is still in progress. G. A. Korn and R. Whigham developed a simple digital-display multiplexer permitting simultaneous display of four digital-logic outputs on a single oscilloscope without analog switching. Reports on these developments will be issued in the course of the academic year 1965/6.

3. Hybrid-code Differential-analyzer Study

The hybrid-code differential-analyzer study was successfully completed with the publication of E. O'Grady's thesis.[1] O'Grady extended J. V. Wait's results by demonstrating various possible tradeoffs between computer accuracy and speed. All the results predicted by H. Skramstad's original theory were borne out by our model; in our judgement, though, the hybrid-code system does not permit enough gain in computing speed to pay for its relative complexity and will probably be overtaken by improved all-digital differential-equation solvers.

References and Publications

During this report period (4/1/65 to 10/1/65), the following new reports were completed:

1. O'Grady, E.: A Hybrid-code Differential Analyzer, ACL Memo No. 87, (M.S. Thesis), April, 1965.

2. Korn, G. A.: Reduction of Digital Noise in Hybrid Analog-digital Computers, ACL Memo No. 114, August, 1965.

The following project reports issued earlier were published or reprinted in journals or conference proceedings during this report period:

3. Hampton, R. L.: Experiments Using Pseudo-random Noise, Simulation, April, 1965.

4. Korn, G. A.: Hybrid-computer Monte-Carlo Techniques, Proc. IFIP Congress, New York, May, 1965; reprinted in Simulation, October, 1965.

5. Whigham, R.: A Fast ±10V Diode Quarter-square Multiplier, Simulation, August, 1965.

6. Mitchell, B. A.: A Hybrid Analog-digital Parameter Optimizer, Simulation, June, 1965 (reprinted from 1964 SJCC Proceedings).

7. Conant, B. K.: ASTRAC I Study of an Orthogonal-function Multiplex System Using Matched Filters, Ann. AICA, July, 1965 (not supported by subject grant, but cited here for reference).

Reprints of these publications are being combined into a fourth University of Arizona Engineering Experiment Station report on the subject study, to be issued in October, 1965.